Application No.: 09/873,580 Docket No.: T2171.0196/P196

AMENDMENTS

In the Claims:

Please amend claims 9 and 18 as follows and add new claims 19-21. Pursuant to the revised format for amendments, the status of each claim is set forth below.

9. (Currently Amended) A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer of non-doped polysilicon onto said gate oxide layer;

patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;

doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said first gate ~~electrodes~~ electrode being doped at a first concentration; and

doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration.

10. (Previously Presented) The method of claim 9, wherein said doping steps comprise implanting ions of an impurity in said first and second active regions and said first and second gate electrodes.

11. (Previously Presented) The method of claim 9, wherein said lower concentration of impurities in said first gate electrode causes the creation of a depletion layer in said first gate electrode when a driving voltage is applied thereto.

12. (Previously Presented) The method of claim 9, wherein said first active region and said first gate electrode are doped simultaneously.

13. (Previously Presented) The method of claim 12, wherein said second active region and said second gate electrode are doped simultaneously.

14. (Previously Presented) The method of claim 12. further including the step of forming a gate oxide under each of said gate electrodes.

15. (Previously Presented) The method of claim 14, wherein both of said gate oxides are the same thickness.

16. (Previously Presented) The method of claim 15, wherein both of said gate oxides have a shape wherein they are thicker at side edges of said gate electrodes than at the center thereof.

17. (Previously Presented) The method of claim 16, further including oxidizing said side walls of said gate electrodes, said gate oxides under each of said gate electrodes being formed while said side walls are oxidized.

18. (Currently Amended) [[A]] The method of ~~manufacturing a semiconductor device comprising at least first and second MOS transistors~~ Claim 9, said method further comprising:

~~providing a semiconductor substrate having at least first and second active regions of a first conductivity type;~~

~~forming a gate oxide layer having a first thickness onto at least said first and second active regions;~~

~~forming an electrode layer onto said gate oxide layer;~~

~~patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;~~

oxidizing sidewalls of said first and second gate electrodes to form an oxide film under said gate electrodes, said oxide film being thicker at said side walls than at a center portion of said gate electrodes[[;]]

~~doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said gate electrodes being doped at a first concentration; and~~

~~doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration~~.

19. (New) The method of claim 11, wherein the depletion region in the gate electrode makes a dielectric breakdown voltage between the gate electrode and the drain region higher.

20. (New) A method of manufacturing a semiconductor device, comprising:

(a) doping a high voltage circuit at a low impurity concentration; and

(b) doping a low voltage circuit at a high impurity concentration after said step (a).

21. (New) The method of claim 21, further comprising:

(c) forming a sidewall spacer after said step (a) and before said step (b).